(Pages : 2) **2006**

Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, May 2014
(2008 Scheme)
08.402 : DIGITAL ELECTRONICS AND LOGIC DESIGN (E)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **four** marks.

1. What do you mean by self -complimenting code ? Give example.
2. Realize a 3 input NAND and NOR using respective 2 input gates.
3. State De-Morgan's theorem and explain.
4. Discuss the difference between combinational and sequential logic circuits.
5. Realize the function , $f = \sum (0, 3, 5, 6)$ using a 4 to 1 multiplexer.
6. What do you mean by purity bit ? Draw the circuit of a 4 - bit parity bit generator.
7. What are the triggering methods of flip-flop ? Explain.
8. Express the given function, $f = (xy + x\bar{z} + yz)$ in standard SOP form.
9. Draw and explain Johnson's counter.
10. Which are the different types of memories ? Give one application to each type.

(10×4=40)

PART – B

Answer **any one** question from **each** Module :

Module – 1

11. Perform the following conversion :
    i) 1762.46_8 to Hexadecimal
    ii) $A08F.EA_{16}$ to Decimal

iii) 158.7_{10} to BCD code

iv) 256.39 to XS-3

v) 1101101_2 to Gray. 20

OR

12. a) Explain weighted and unweighted codes. 5

b) Simplify the following Boolean function using K-map in POS form and realize the function using NOR gates only. 15

$F = (A, B, C, D) = A\overline{B}C + \overline{B}C\overline{D} + BCD + AC\overline{D} + \overline{A}\overline{B}C + \overline{A}B\overline{C}D$.

Module – 2

13. a) Describe the working of a full adder. Design and draw full adder using 2 half adders and an OR gate. 10

b) Draw and explain a 4-bit magnitude comparator. 10

OR

14. a) Give the internal circuit circuitry of CMOS NAND gate and explain its all conditions of operation. 10

b) Design and explain BCD to 7 segment decoder. 10

Module – 3

15. a) Explain Race-around condition of J-K Flip. Draw the circuit of Master-slave flip-flop and explain its working. 10

b) Design and draw the circuit of a 3-bit synchronous up counter. 10

OR

16. a) Classify shift register. Draw and explain the operation of a parallel in-serial out shift register. 10

b) Design an astable multivibrator using 555 having 1 kHz frequency and duty cycle of 0.6. Draw the circuit diagram. 10

(3×20=60)